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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,585	02/24/2004	Inyup Kang	030374	4356

23696 7590 06/15/2007
QUALCOMM INCORPORATED
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EXAMINER

NGUYEN, SIMON

ART UNIT	PAPER NUMBER
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2618

NOTIFICATION DATE	DELIVERY MODE
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06/15/2007

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/786,585

Applicant(s)

KANG ET AL.

Examiner

SIMON D. NGUYEN

Art Unit

2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 April 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-7, 9, 11-18, 21, 23-24, 26-31, 34-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al (2003/0133337 A1) in view of Nonogaki (6,625,478).

Regarding claim 1, Yamada discloses an integrated circuit (semiconductor device) for a wireless communication device (a cellular phone) (paragraphs 3, 5, figs. 2, 7), comprising: an always-on power domain (A) including circuit blocks (11, 12) coupled to a first power supply (POWER SUPPLY) and powered on at all times (paragraph 45); and collapsible power domains (B, C), each collapsible power domain including circuit blocks ((13, 13a, 13b, 14, 14a) or (15, 15a, 16) coupled to a second power supply (first and second power supplies are the same as claimed in claim 7) via a respective power connection (via switches 17, 18) and powered on/off by the power connection (paragraph 48), wherein the always-on power domain determines power on and off states of all of the collapsible power domain (paragraphs 33, 42). However, Yamada

fails to teach the always-on power domain determines independently power on/off states of all of the collapsible power domains.

Nonogaki discloses a wireless phone having an always-on power domain (101) coupled to a power supply (103), wherein the always-on power domain determines independently power on/off states of all of collapsible power domains (200, 300, 400) via switches 104, 105, 106 respectively (fig.1). Therefore, it would have been obvious to one skilled in the art at the time the invention was made in order to directly control a power supply for each portion of a wireless phone.

Regarding claim 23, this claim is rejected for the same reason as set forth in claim 1, Yamada discloses a cellular phone comprising a modem processor (A) to perform demodulation for the cellular phone (paragraphs 3, 5, figs. 2, 7), wherein the modem comprising: an always-on power domain (A) including circuit blocks (11, 12) coupled to a first power supply (POWER SUPPLY) and powered on at all times (paragraph 45); and collapsible power domains (B, C), each collapsible power domain including circuit blocks ((13, 13a, 13b, 14, 14a) or (15, 15a, 16) coupled to a second power supply (first and second power supplies are the same as claimed in claim 7) via a respective power connection (via switches 17, 18) and powered on/off by the power connection (paragraph 48), wherein the always-on power domain determines power on and off states of all of the collapsible power domain (paragraphs 33, 42). wherein Nonogaki discloses the wireless phone, wherein the wireless phone comprising a modulator, a demodulator, a controller (fig.1).

Regarding claims 27 and 34, these claims are rejected for the same reason as set forth in claim 1.

Regarding claim 2, Yamada discloses a method for controlling power in a cellular phone, comprising one collapsible power domain for demodulating (13). It should be noted that a transmitter includes a modulator is inherently in a cellular phone. However, Yamada does not specifically disclose a collapsible power domain for a modulator.

Nonogaki discloses a method for controlling collapsible power to a transmitter and a receiver (312, 313 of block 300 of fig.1) wherein the transmitter inherently includes a modulator (fig. 1). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have Yamada, modified by Hattori to cut off power supply to a transmitter when the phone is not in a transmission mode in order to save power.

Regarding claims 3-4, 24, Yamada further discloses a timing chart for controlling sleep or active times to each parts of the phone and the receiving part is power off when it does not receive a message signal (figs. 4, 6, paragraphs 51-65).

Regarding claims 5-6, Yamada further discloses each collapsible having a switch for turning on/off the power supply, wherein the switch Yamada is considered as head-switch (17, 18 of fig. 2).

Regarding claim 7, Yamada further discloses the first and second power supplies are one common power supply (paragraph 48).

Regarding claim 9, Yamada further discloses the CPU as a power controller for controlling a control signal to power on/off the collapsible power domains (fig. 2, paragraphs 45-46).

Regarding claims 11-12, Yamada further discloses a sleep mode (fig.3) which means the power control including a sleep controller (paragraph 53) and a clock control (timer part 12) to control timing for turning on/off the parts B, C (paragraphs 45-52).

Regarding claims 13-14, Yamada further discloses output circuits (17, 18) for at least one output pin (wherein the output pin is where the power supply entered into the switch) of the integrated circuit (A) (switches 17, 18), each output circuit receiving an output signal from one of the collapsible power domain (connected from either B or C to the switch) (fig.2), wherein each output circuit includes a latch to maintain logic state of the output signal (fig.8).

Regarding claim 15-16, Yamada discloses switches 17, 18 for connecting always-on power supply part A to the collapsible parts B, C, wherein the switching part is considered as an interface (fig.2), or a line from the power supply to other parts 2, 3 via a switch 8 is considered as an interface (fig.1), wherein Yamada further discloses a clamping circuit (31) for clamping power to logic low or high and a level shifter (32) to translate between two different voltages (fig.8).

Regarding claim 18, Yamada further discloses a register for storing instructions, wherein the register is in the integrated circuit (fig.5, paragraphs 56, 59, 63) wherein the instruction for power supply in a CDMA is inherently a coding instruction

Regarding claim 21, Yamada further discloses the device is a CDMA system (paragraph 74).

Regarding claims 26, 31, Yamada further discloses a memory (register) for storing program code (instruction), placed in a self-refresh mode (boot process and restored) (paragraphs 59, 63-65).

Regarding claims 28-30, 35-36, Yamada further discloses the steps of receiving an indication to enter sleep and powering off one of the collapsible power domain (paragraph 54); latching logic states and releasing output pins (paragraphs 69-45, fig.8) (It should be noted pins are inherently in an on-chip semiconductor); saving and restoring the hardware states when it is powered on/off (paragraph 65).

Regarding claim 37, Yamada further discloses the always-on power domain independently determined power on/off state of each of the collapsible power domain (paragraph 42).

Regarding claims 38-39, Yamada further discloses sequentially powering on/off the integrated circuit (paragraphs 40, 41).

Regarding claim 17, Yamada further discloses each power switch (17 or 18) including a transistor (wherein the transistor combined by a plurality of diodes) for switch on/off power supply to the collapsible parts (fig.8). it should be noted that in order to prevent shorting of power supply the sufficient number of electrostatic discharge diodes is a much in the transistor which is known to those skilled in the art.

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3. Claims 8, 10, 22, 25, 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al (2003/0133337 A1) in view of Nonogaki (6,625,478) as applied to claim 1, and further in view of Grayson et al. (6,219,564).

Regarding claim 8, Yamada fails to disclose two different power supplies.

Grayson discloses a cellular phone having two different power supplies (11, 27 of fig.1), which supply different voltages (column 2 lines 28-34, 58-65). Therefore, it would have been obvious to have modified Yamada, modified by Grayson in order to prevent disable of the phone when one power supply is defected.

Regarding claim 10, Yamada discloses the power control turns on the switches 17, 18 for the collapsible power domains B, C when a message is detected by incoming call determination part 14a and turns off when the incoming call determination part 14a does not detect any incoming signal (paragraphs 54-55), which is obvious the power control includes an interrupting controller. However, Yamada does not specifically say so.

Grayson discloses an interrupt control unit (CPU) for interrupting power to other parts of the phone as a way to save power when it is not in active (column 3 lines 33-65). Therefore, it would have been obvious to have Yamada, modified by Grayson in order to conserve power.

Regarding claim 22, Yamada discloses the device used in a CDMA system. However, Yamada fails to disclose used in a GSM.

Grayson discloses the power control used in a GSM system (column 1 lines 6-7). Therefore, it would have been obvious to have Yamada, modified by Grayson in order to converse power for a GSM mobile device.

Regarding claim 25, Yamada fails to disclose two oscillators.

Grayson discloses a mobile device having two oscillators one is a main oscillator, another is for a sleep mode (column 2 line 66 to column 3 line7).

Regarding claims 32-33, Yamada fails to disclose disabling/enabling clocks and power off/on an oscillator.

Grayson discloses de-activating/re-activating clocks (page 1 lines 21-35) and power on/off the oscillator (column 3 line 3). Therefore, it would have been obvious to have Yamada, modified by Grayson in order to converse power of the battery.

4. Claims 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al (2003/0133337 A1) in view of Nonogaki (6,625,478) as applied to claim 1, and further in view of Foster et al. (6,715,085).

Regarding claims 19-20, these claims are rejected for the same reason as set forth in claim 1. However, Yamada fails to teach a boot code for configuring a memory system for the integrated circuit downloaded from an external non-volatile memory to the internal memory.

Foster discloses an integrated system in which an internal memory receives boot code for configuring a memory system for the integrated system, wherein the boot code is downloaded from an external non-volatile memory to the internal memory and used to

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executed the integrated system (column 9 lines 6-35). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have modified Yamada, modified by Foster to easily update the new programming code in order to improve the system performance.

Response to Arguments

5. Applicant's arguments with respect to independent claims 1, 19, 20, 23, 27, 34 have been considered but are moot in view of the new ground(s) of rejection.

The new cited art issued to Nonogaki (6,625,478) discloses the always-on power domain 101 independently determines power on/off states of all collapsible power domains 200, 300, 400 (fig.1) and Nonogaki further discloses the wireless phone is an integrated circuit (column 6 lines 32-33) which means the switches 104, 105, 106, power management controller 101 and all other parts 200, 300, 400 included inside the integrated circuit.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Simon Nguyen whose telephone number is (571) 272-7894. The examiner can normally be reached on Monday-Friday from 7:00 AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban, can be reached on (571) 272-7899.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 306-0377.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
600 Dulany, Alexandria, VA 22314

Or faxed to:

(571) 273-8300 (for formal communications intended for entry)

Hand-delivered response should be brought to Customer Service Window
located at the Randolph Building, 401 Dulany, Alexandria, VA, 22314.

Simon Nguyen

June 6, 2007

A handwritten signature in black ink, appearing to read 'Nguyen', with a large, stylized initial 'S' on the left.

**SIMON NGUYEN
PRIMARY EXAMINER**